What is claimed is:

1. A jitter detecting circuit detecting a jitter value of a signal which is converted into a digital signal from an analog signal input, wherein the jitter detecting circuit comprises:

an edge detector discriminating signs of two signals derived from consecutive sampling points from the digitally converted input signal, and outputting the two signals as first and second edge signals, respectively, if the signs are different from each other;

a comparator outputting a signal having a smaller absolute value among the first and second edge signals output from the edge detector;

an operating unit dividing the absolute value output from the comparator by a sum of the absolute value of the first edge signal and that of the second edge signal; and

an accumulator accumulating outputs of the operating unit during a predetermined period, to obtain a jitter value of the predetermined period.

2. The jitter detecting circuit of claim 1, wherein the edge detector comprises:

a delayer delaying the digitally converted input signal by one system clock; and

an edge generator comparing signs of the delayed digitally converted input signal with signs of the digitally converted input signal, and outputting the two signals as the first edge signal and the second edge signal, respectively, if the signs are different with respect to each other.

3. The jitter detecting circuit of claim 2, wherein the edge generator comprises:

a first bit detector detecting a most significant bit of the digitally converted input signal;

a second bit detector detecting a most significant bit of the delayed digitally converted input signal ;

an exclusive OR calculator performing an exclusive-OR operation on the extracted most significant bits of the first bit detector and the second bit detector;

a first edge signal generator using the output value of the exclusive OR calculator as a clock signal, and using the digitally converted input signal to generate the first edge signal; and

a second edge signal generator using the output value of the exclusive OR calculator as a clock signal simultaneously with the first edge signal generator, and using the digital input signal through the delayed digitally converted input signal, to generate the second edge signal.

4. A digital phase locked loop comprising:

a jitter signal generator comprising:

an edge detector generating first and second edge signals by discriminating sign changes from consecutive sampling points from a digital converted input signal,

a comparator outputting a signal having a smaller absolute value among the first and second edge signals output from the edge detector , and

an operating unit dividing the absolute value output from the comparator by a sum of the absolute value of the first edge signal and that of the second edge signal to obtain a jitter signal ; and

a phase locked signal generator generating a phase locked signal, using the jitter signal generated from the jitter signal generator as a phase error signal.

5. A jitter detecting circuit to detect jitter from analog signal converted to a digital signal, comprising:

an edge detector detecting edges of the digital signal by determining when signs of consecutive sample points of the digital signal are different from each other, and in response, outputting first and second edge detection signals; and

a jitter determining circuit determining the jitter from the first and second edge detection signals.

6. The jitter detecting circuit of claim 5, wherein the jitter determining circuit comprises an accumulator accumulating the jitter over a predetermined time, to generate a jitter value for the predetermined time.

7. A method of determining a jitter value comprising:

determining two sampling points of a digitally converted analog signal;

dividing the sampling cycle between the two sampling points by the sum of the amplitudes of the two sampling points; and

multiplying the smaller sample point amplitude by the divided amount.

8. A method of detecting a jitter value comprising:

converting an analog signal to a digital signal;

checking consecutive sampling points from the digitally converted signal; and

calculating the jitter value using the sampling points.

9. The method of claim 8, wherein the calculating the jitter value comprises:

discriminating signs of the two sampling points;

obtaining first and second edge signals from the two sampling points if the signs are different;

dividing the smaller absolute value of the first edge signal and the second edge signal by a sum of the absolute value of the first edge signal and the second edge signal.

10. The method of claim 9, wherein the obtaining first and second edge signals comprises:

delaying the digitally converted signal by one clock signal;

comparing a sign of the digitally converted signal with a sign of the delayed digitally converted signal; and

outputting the digitally converted signal and the delayed digitally converted signal as first and second edge signals if the signs are different.

11. A method of providing a phase locked signal comprising:

generating first and second edge signals by discriminating a sign change from consecutive sampling points from a digitally converted analog signal;

outputting a signal having a smaller absolute value among the first and second edge signals generated;

generating a jitter signal by dividing the smaller absolute value of the first edge signal and the second edge signal by a sum of the absolute value of the first edge signal and the second edge signal; and

using the jitter signal as a phase error signal.